REMARKS

Claims 1-29 were pending in the application. Claims 7 and 29 have been cancelled. Claim 30 has been added. Claims 8-20 and 28 have been amended. Accordingly, Claims 1-6, 8-28, and 30 are now pending in the application.

35 U.S.C. §102 Rejection

Claims 1-29 were rejected under 35 U.S.C. 102(e) as being anticipated by Zadikian et al. (U.S. Patent No. 6,724,757).

1. Applicant respectfully submits that Zadikian fails to teach or suggest, "wherein the server shelves are logically connected into a plurality of stacks, wherein the switching modules of the respective shelves in each stack are interconnected in a logical stacking configuration" as recited by claim 1.

On pages 2 and 4 of the pending Office Action, the Examiner contends that column 9, lines 25-42, column 10, lines 10-27, column 11, line 45 – column 13, line 36, and Figures 1A, 2-4 of Zadikian teach the above-highlighted features of claim 1. Applicant respectfully disagrees.

As shown in FIG. 4 of Zadikian, the router system includes various shelves, each shelf including 16 slots that are divided into four functional groups. Three of the four functional groups are made up of line cards 220 and occupy 5 slots each for a total of 15 slots. (*See* Zadikian at column 12, lines 45-49). In each line card group, four of the five slots include I/O line cards and the fifth slot includes line cards containing a switching matrix for the group and a hub (e.g., an Ethernet hub). (*See id.* column 12, lines 61-65 and column 13, lines 6-8). The fourth functional group occupies a single slot and includes the shelf processor. (*See id.* column 12, lines 49-51). Thus, each shelf includes I/O line cards, switch cards, and a shelf processor card. (*See id.* column 12, lines 51-57).

At column 11, line 45 – column 12, line 7, Zadikian discloses:

> FIG. 3 also illustrates certain features of router 100 pertaining to the relationship between shelf switches 320(1)-(N) and 321(1)-(N), and groups 310(1)-(N). Groups 310(1)-(N) are again shown, with regard to the control functions thereof. In this depiction of groups 310(1)-(N), line cards 220(1,1)-(N,N) are shown as being attached to networking devices, indicated here as group matrices. Group matrices 212(1)-(N) and 216(1)-(N) may be, for example, multi-port Ethernet hubs running at 10 Mbps. Each of line cards 220(1,1)-(N,N) feed signals into two of group matrices 212(1)-(N) and 216(1)-(N). For example, line card 220(1,1) feeds received information to group matrix 212(1) and group matrix 216(1). Group matrices 212(1)-(N) and 216(1)-(N) each feed a signal into shelf switches 320(1)-(N) and 321(1)-(N) of FIG. 2. Shelf switches 320(1)-(N) and 321(1)-(N) are each controlled by a shelf processor (not shown), for the sake of clarity and communicate with one of the system switches (not shown, for the sake of clarity).
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> Shelf switches 320(1)-(N) and 321(1)-(N) are the next higher level of the control hierarchy in router 100, and are located on the shelf processor module (exemplified by line racks (330(1)-(N)). Each copy of shelf switches 320(1)-(N) and 321(1)-(N) interconnects six connections from the three groups in **each shelf**, another connection from the shelf processor, and one connection from system switch 340 (and 341). Shelf switches 320(1)-(N) and 321(1)-(N) can be implemented, for example, using an 8-port Ethernet configured to handle 10 Mbps Ethernet traffic and a single-port, dual-rate switch (e.g., 10 Mbps/100 Mbps Ethernet). (Emphasis added)

Zadikian discloses that each shelf switch 320 interconnects three functional I/O groups in each shelf (via the corresponding group matrices 212, 216), connects to the corresponding shelf processor, and further connects to the system switch 340. (*See* Zadikian at column 12, lines 54-63 and column 13, lines 1-4)

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). (Emphasis added)

As noted above, in Zadikian, each group matrix 212, 216 and each shelf switch 320 interconnect modules from functional groups located within a single shelf. (*See* Zadikian at column 11, line 45 – column 12, line 7 and column 12, line 44 – column 13, line17). However, Applicant respectfully submits that Zadikian fails to teach, "wherein the server shelves are logically connected into a plurality of stacks, wherein the switching modules of the respective shelves in each stack are interconnected in a logical stacking configuration" as recited by claim 1. In other words, Zadikian fails to disclose that each **shelf** of the router system is "logically connected into a plurality of stacks" and fails to disclose that the "switching modules" in the shelves of the Zadikian system "in each stack are interconnected in a logical stacking configuration" (see claim 1). In Zadikian, although the cards within each shelf are divided into functional groups, the shelves themselves are not "connected into a plurality of stacks."

2. Applicant further submits that Zadikian fails to teach or suggest, "wherein the master switching module is connected into each stack as a common master switch for all of the stacks, wherein the master switching module is connected to the switching module of a first server shelf and to the switching module of a last server shelf in each of the stacks" as recited by claim 1.

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). (Emphasis added)

While Zadikian discloses, "Each of line cards 220(1,1)-(N,N) feed signals into two of group matrices 212(1)-(N) and 216(1)-(N)" and "Group matrices 212(1)-(N) and 216(1)-(N) each feed a signal into shelf switches 320(1)-(N) and 321(1)-(N)" (*See* Zadikian at column 12, lines 54-56 and 58-60), Zadikian fails to teach, "wherein the master switching module is connected into each stack as a common master switch for all

of the stacks, wherein the master switching module is connected to the switching module of a first server **shelf** and to the switching module of a last server **shelf** in **each** of the stacks" as recited by claim 1. In Zadikian, a shelf switch 320 interconnects modules from functional groups located within a single shelf, and system switch 340 is connected to all the shelf switches 320. (*See* Zadikian at column 11, line 45 – column 12, line 7 and column 12, line 44 – column 13, line17). Zadikian, however, does not teach that a shelf switch 320 or system switch 340 "is connected to the switching module of a first server **shelf** and to the switching module of a last server **shelf** in **each** of the stacks" as recited by claim 1. In fact, as noted above, Zadikian fails to teach the concept of "stacks" (see claim 1, i.e., "wherein the server shelves are logically connected into a plurality of stacks, wherein the switching modules of the respective shelves in each stack are interconnected in a logical stacking configuration").

Accordingly, claim 1 is believed to patentably distinguish over Zadikian. Claims 2-6 and 8-27 are dependent upon claim 1 and are therefore believed to patentably distinguish over the cited reference for at least the same reasons.

Likewise, claim 28 recites features similar to those highlighted above with regard to claim 1 and is therefore believed to patentably distinguish over Zadikian for at least the reasons given in the above paragraphs discussing claim 1.

3. Applicant respectfully requests examination of added claim 30. Applicant submits that claim 30 recites features similar to those highlighted above with regard to claim 1 and is therefore believed to patentably distinguish over Zadikian for at least the reasons given in the above paragraphs discussing claim 1.

Furthermore, Applicant submits that Zadikian fails to teach or suggest, "wherein the server shelves are logically connected into a plurality of stacks, wherein each stack includes two or more server shelves, wherein for **each stack** at least one switching module removably received in a server shelf of the stack is interconnected with at least one switching module removably received in a **separate** server shelf of the **same stack**"

as recited by claim 30. Accordingly, claim 30 is believed to patentably distinguish over Zadikian.

4. Applicant also asserts that numerous ones of the dependent claims recite further distinctions over the cited art. For instance:

5. Applicant submits that Zadikian fails to teach, "wherein the information processing modules are configured as server blades and are further configured as field replaceable units, and wherein the master switch module is also configured as a field replaceable unit" as recited by claim 8. Accordingly, claim 8 is believed to patentably distinguish over Zadikian.

6. Applicant submits that Zadikian fails to teach, "wherein each server shelf comprises two switching modules removably received therein, wherein the server shelves are logically connected into a plurality of stacks, wherein the switching modules of the respective shelves in each stack are interconnected in at least one logical stacking configuration, wherein each stack includes two or more server shelves, wherein for each stack the two switching modules removably received in at least one server shelf of the stack are interconnected with the two switching modules removably received in a **separate** server shelf of the **same** stack, wherein the computer system further comprises a master shelf including a carrier for removably receiving two master switching modules, wherein each of the master switching modules is connected into each stack as a common master switch for all of the stacks, wherein a first of the master switching modules is connected to a first switching module of a first server shelf and to a first switching module of a last server shelf in each of the stacks, and wherein a second of the master switching modules is connected to a second switching module of a first server shelf and to a second switching module of a last server shelf in each of the stacks" as recited by claim 18. Accordingly, claim 18 is believed to patentably distinguish over Zadikian.

7. Applicant submits that Zadikian fails to teach, "wherein each switching module of each server shelf comprises a service processor module" as recited by claim 20.

Accordingly, claim 20 is believed to patentably distinguish over Zadikian.

8. Applicant submits that Zadikian fails to teach, "wherein each controlling element is operable to control the operation of the forwarding element to cause a unicast data element to be forwarded by its respective forwarding element using a shortest transmission path to its target" as recited by claim 24. Accordingly, claim 24 is believed to patentably distinguish over Zadikian.

9. Applicant submits that Zadikian fails to teach, "wherein each controlling element is operable to control the operation of the forwarding element to cause a multicast or broadcast data element to be forwarded once around the stack in a given direction" as recited by claim 25. Accordingly, claim 25 is believed to patentably distinguish over Zadikian.

10. Applicant submits that Zadikian fails to teach, "wherein the controlling element is operable to study a transmitted data element to determine a path to destination based on the content of that data element" as recited by claim 27. Accordingly, claim 27 is believed to patentably distinguish over Zadikian.

CONCLUSION

Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-70900/MJL.

Respectfully submitted,

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